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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,144	08/27/2004	Douglas D. Coolbaugh	BUR920040107US1	5143

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,144	COOLBAUGH ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/27/04; 09/03/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, Claims 1-14 in the reply filed on July 20th, 2006 is acknowledged.

Oath/Declaration

2. The oath/declaration filed on August 27th, 2004 is acceptable.

Information Disclosure Statement

3. The Information Disclosure Statement filed on August 27th, 2004 and September 3rd, 2004 has been considered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 4 recites the limitation "said second doped region" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

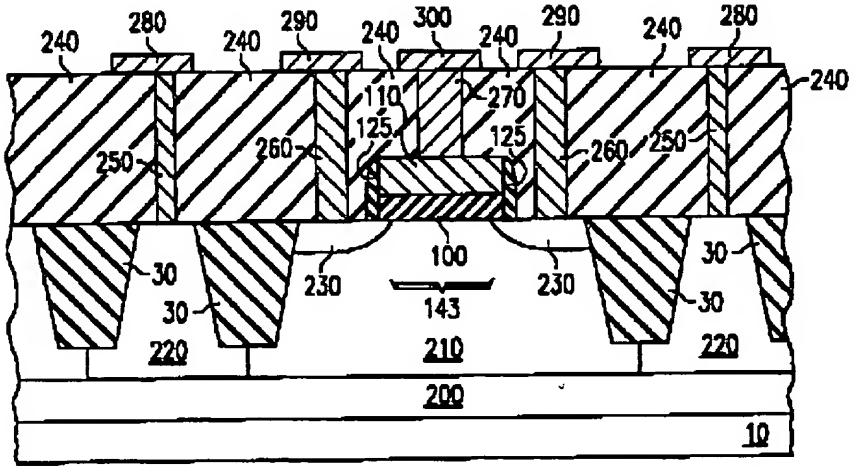
6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Benaissa et al. (U.S. Patent 7,053,465).

In re claim 1, **Benaissa** discloses a varactor structure comprising: a semiconductor substrate 10 of a first conductivity type (p-type) (col. 2, lines 15-16), the substrate 10 including a doped region 200 of a second conductivity type (n-type) (col. 4, line 52) located below an upper region 143 (col. 5, lines 4-5) of the substrate 10, the first conductivity type (p-type) is different from the second conductivity type (n-type); a well region located in the upper region 143 of the substrate 10, wherein the well region includes outer well regions 220 of the second conductivity type (n-type) (col. 4, lines 57-58) and an inner well region 210 of the first conductivity type (p-type) (col. 4, lines 56-57), each well of the well region is separated at an upper surface by an isolation region 30 (col. 4, lines 50-51); and a field effect transistor having at least a gate conductor 110 of the first conductivity type (col. 4, lines 60-61) located above the inner well region 210 (col. 4, line 47 to col. 5, line 10 and FIG. 4).

FIG. 4



In re claim 2, as applied to claim 1 above, **Benaissa** discloses all claimed limitations including the limitation wherein the first conductivity type comprises a p-type dopant and second conductivity type comprises a n-type dopant (col. 4, lines 56-57).

In re claim 3, as applied to claim 1 above, **Benaissa** discloses all claimed limitations including the limitation wherein the first conductivity type comprises a n-type dopant and the second conductivity type comprises a p-type dopant (col. 4, lines 56-57).

In re claim 4, as applied to claim 1 above, **Benaissa** discloses all claimed limitations including the limitation wherein the second doped region 200 is a subcollector or an isolation well (col. 4, lines 50-51 and FIG. 4).

In re claim 5, as applied to claim 1 above, **Benaissa** discloses all claimed limitations including the limitation wherein each well region extends beneath the isolation region 30 such that neighboring well regions 210, 220 are in contact with each other (col. 4, lines 53-58 and FIG. 4).

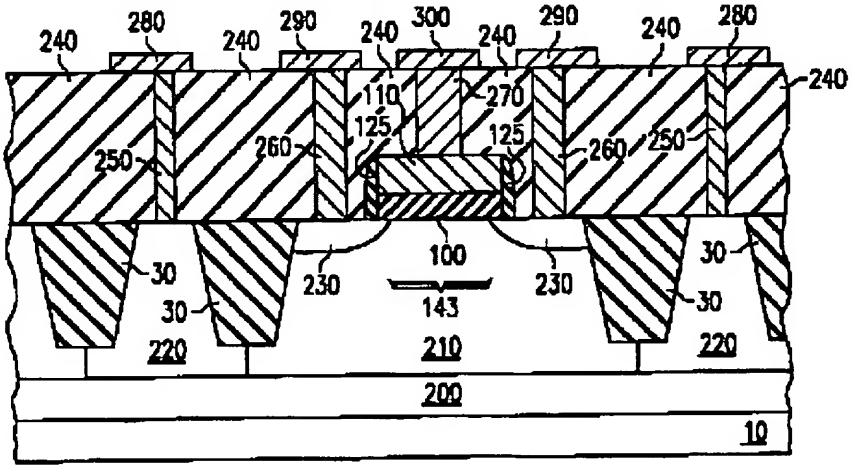
In re claim 6, as applied to claim 1 above, **Benaissa** discloses all claimed limitations including the limitation wherein the upper region 143 of the substrate 10 comprises an epitaxial semiconductor layer (col. 5, lines 2-10).

In re claim 7, as applied to claim 1 above, **Benaissa** discloses all claimed limitations including the limitation wherein the field effect transistor further comprises a gate dielectric 100located beneath the gate conductor 110, a hard mask located on the gate conductor, at least one spacer 125 located on sidewalls of the gate conductor 110 and abutting source/drain regions 230 (col. 4, lines 60-66 and FIG. 4).

In re claim 8, as applied to claim 1 above, **Benaissa** discloses all claimed limitations including the limitation wherein the gate conductor 110 comprises polysilicon (col. 2, lines 40-41).

In re claim 9, **Benaissa** discloses a varactor structure comprising a p-type semiconductor substrate 10 (col. 2, lines 15-16), the p-type substrate including an n-doped region 200 (col. 4, line 52) located below an upper region 143 (col. 5, lines 4-5) of the substrate 10; a well region located in the upper region 143 of the substrate 10, wherein the well region includes outer N-well regions 220 (col. 4, lines 57-58) and an inner P-well region 210 (col. 4, lines 56-57), each well of the well region is separated at an upper surface by an isolation region 30 (col. 4, lines 50-51); and a field effect transistor having at least a p-type gate conductor 110 (col. 4, lines 60-61) located above the inner P-well region 210 (col. 4, line 47 to col. 5, line 10 and FIG. 4).

FIG. 4



In re claim 10, as applied to claim 9 above, **Benaissa** discloses all claimed limitations including the limitation wherein the n-doped region 200 comprises a subcollector or an isolation well (col. 4, lines 50-51 and FIG. 4).

In re claim 11, as applied to claim 9 above, **Benaissa** discloses all claimed limitations including the limitation wherein each well region extends beneath the isolation region 30 such that neighboring well regions 210, 220 are in contact with each other (col. 4, lines 53-58 and FIG. 4).

In re claim 12, as applied to claim 9 above, **Benaissa** discloses all claimed limitations including the limitation wherein the upper region 143 of the substrate 10 comprises an epitaxial semiconductor layer (col. 5, lines 2-10).

In re claim 13, as applied to claim 9 above, **Benaissa** discloses all claimed limitations including the limitation wherein field effect transistor further comprises a gate dielectric 100 located beneath the gate conductor 110, a hard mask located on the gate conductor 110, at least one spacer 125 located on sidewalls of the gate conductor 110 and abutting source/drain regions 230 (col. 4, lines 60-66 and FIG. 4).

In re claim 14, as applied to claim 9 above, **Benaissa** discloses all claimed limitations including the limitation wherein the gate conductor comprises polysilicon (col. 2, lines 41-42).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K.N.
August 06, 2006

MATTHEW SMITH
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